REMARKS

This Amendment is submitted in answer to the Office Action dated February 27, 2009, having a shortened statutory period set to expire May 27, 2009.

I. Amendment to the specification

Applicant has proposed an amendment to rewrite the title of the present application. In addition, Applicant has supplied the application serial number omitted from paragraph [0001] of the present specification, as suggested by the Examiner. The proposed amendments to the specification do not contain any new matter, and entry of the amendments is respectfully requested.

II. Replacement drawing sheet

Upon review of Figure 5A, Applicant noted a draftsman's error in preparing the formal drawings, namely, an erroneous arrow connecting block 114 to block 120 (which was absent in the originally filed drawing). Accordingly, Applicant has submitted a replacement drawing sheet to correct this error. The replacement drawing sheet does not contain any new matter.

III. Rejection under 35 U.S.C. § 103

At page 2 of the present Office Action, Claims 1-18 are rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,697,919 to *Gharachorloo et al.* (*Gharachorloo*) in view of U.S. Patent Publication No. 2003/0120881 to *Lai et al.* (*Lai*). That rejection is respectfully traversed, and favorable reconsideration of the claims is requested.

A. Combination of *Gharachorloo* and *Lai* does not disclose the speculative memory access recited in exemplary independent Claim 1

The combination of *Gharachorloo* and *Lai* does not render exemplary Claim 1 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose a memory controller that performs speculative memory access as recited in exemplary Claim 1 as amended:

> ... wherein said memory controller, responsive to receipt of a memory access request broadcast to the memory controller and the plurality of cache memories:

> if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing said system memory; and
>
> if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory.

At indicated at page 7 of the present Office Action, the combination of *Gharachorloo* and *Lai* discloses a page-table register unit that tracks addresses of previous memory access requests, and if an address match occurs for a next memory access request, enables precharge of the memory during a current access to reduce access latency. See, e.g., *Lai*, paragraphs [0017] and [0029]. However, the combination of cited references does not disclose or suggest different timings of access to system memory relative to a coherency message based upon a memory speculation mechanism, as claimed. Consequently, Applicant respectfully submits that the rejection of exemplary Claim 1, similar Claims 9 and 14, and their respective dependent claims under 35 U.S.C. § 103 is overcome.

B. Combination of *Gharachorloo* and *Lai* does not disclose the features recited in exemplary dependent Claim 3

The combination of *Gharachorloo* and *Lai* also does not render exemplary Claim 3 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features of Claim 3:

> ... said memory speculation mechanism comprises a memory speculation table that stores a respective memory access history for each of a plurality of threads executing within said one or more processing cores.

At pages 4 of the present Office Action, the Examiner relies upon *Gharachorloo's* disclosure of a cache directory 180, instruction-level parallelism, simultaneous multithreading (SMT), and out-of-order execution as teaching the features of Claim 3. Applicant respectfully traverses the Examiner's position because none of these features of *Gharachorloo's* processor cores discloses a memory speculation table of a memory controller that stores a per-thread history, as required by the

recitation that the "memory speculation table stores a respective memory access history for each of a plurality of threads executing within said one or more processing cores." Because the combination of *Gharachorloo* and *Lai* does not disclose the features recited in exemplary Claim 3, Applicant respectfully submits that the rejection of exemplary Claim 3 and similar Claims 10 and 15 under 35 U.S.C. § 103 is overcome.

C. Combination of *Gharachorloo* and *Lai* does not disclose the features recited in exemplary dependent Claim 4

The combination of *Gharachorloo* and *Lai* also does not render exemplary Claim 4 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features of Claim 4:

> ... said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said memory speculation mechanism stores said historical information on a per-bank basis.

At page 4 of the present Office Action, the Examiner relies, *inter alia*, upon *Gharachorloo's* disclosure of memory banks as teaching the features of Claim 4. Applicant respectfully traverses the Examiner's position because *Gharachorloo's* disclosure of memory banks does not disclose a memory speculation table of a memory controller that stores a per-bank history, as required by Claim 4. Further, *Lai* teaches that the access history relied upon by the Examiner is not stored on a per-bank basis, but rather for precise memory addresses. Because the combination of *Gharachorloo* and *Lai* does not disclose the features recited in exemplary Claim 4, Applicant respectfully submits that the rejection of exemplary Claim 4 and similar Claims 11 and 16 under 35 U.S.C. § 103 is overcome.

D. Combination of *Gharachorloo* and *Lai* does not disclose the features recited in exemplary dependent Claim 5

The combination of *Gharachorloo* and *Lai* also does not render exemplary Claim 5 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features of Claim 5:

> ... wherein said coherency message comprises a combined response representing a

systemwide response to said memory access request.

At page 4 of the present Office Action, the Examiner relies upon *Gharachorloo's* column 7 as disclosing a memory controller speculatively initiating access to system memory and further relies upon col. 11, line 19 as teaching that the access is made prior to receipt of the combined response. Applicant respectfully traverses the Examiner's position because *Gharachorloo's* column 7 nowhere discloses a memory controller, such as *Gharachorloo's* memory controller 118, speculatively initiating access to system memory. Further, col. 11, line 19 merely discloses the execution of instructions from a microcode array "to advance memory transactions," but completely fails to disclose that the coherency message (of Claim 1) is a combined response for the memory access request, as recited by Claim 5. Because the combination of *Gharachorloo* and *Lai* does not disclose the features recited in exemplary Claim 5, Applicant respectfully submits that the rejection of exemplary Claim 5 and similar Claim 17 under 35 U.S.C. § 103 is overcome.

E. Combination of *Gharachorloo* and *Lai* does not disclose the features recited in exemplary dependent Claim 6

The combination of *Gharachorloo* and *Lai* also does not render exemplary Claim 6 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features of Claim 6:

> ... said memory controller speculatively initiates access to said first system memory based upon historical information recorded by said second memory controller.

At page 5 of the present Office Action, the Examiner relies upon *Gharachorloo's* column 21, lines 59-63 as disclosing that *Gharachorloo's* cache coherence protocol enables sharing of memory lines across multiple nodes. Applicant respectfully traverses the Examiner's position because *Gharachorloo's* disclosure of a coherency protocol fails to disclose the speculative initiation of access to a system memory by a first system memory controller based upon historical information recorded by a second memory controller, as recited by Claim 6. Because the combination of *Gharachorloo* and *Lai* does not disclose the features recited in exemplary Claim 6, Applicant respectfully submits that the rejection of exemplary Claim 6 and similar Claims 13 and 18 under 35 U.S.C. § 103 is overcome.

F. Combination of *Gharachorloo* and *Lai* does not disclose the features recited in new Claims 19-24

The combination of *Gharachorloo* and *Lai* also does not render new Claims 19-24 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features recited therein:

> ... wherein the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory as indicated by the coherency message.

or

> ... wherein the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request.

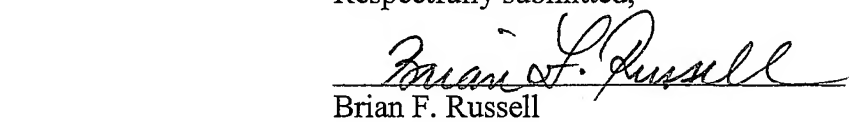
Because the combination of *Gharachorloo* and *Lai* does not disclose the features recited in new Claims 19-24, Applicant respectfully submits that these claims are not rendered unpatentable by the cited combination of references under 35 U.S.C. § 103.

IV. CONCLUSION

Having now addressed and overcome each outstanding rejection, Applicant respectfully submits that all claims now pending are in condition for allowance and respectfully requests such allowance.

Please charge any fee necessary to further the prosecution of this application to IBM Corporation Deposit Account No. **09-0447**.

Respectfully submitted,



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